# NRM1

# Hardware Manual

## Contents

➢ Revision History

All revisions made to this document are listed below;

| Version | Date | Description |
|---|---|---|
| 0.1 | 2022-02 | 문서 초안 작성 |
| 0.2 | 2022-07 | If I2C interface are used, 2.2K Ω pull-up registers are required in the customer board. |
| 0.3 | 2022-10 | Memory spec was changed from 4Gbit NAND Flash + 4Gbit LPDDR4 to 8Gbit NAND Flash + 8Gbit LPDDR4 |
| | | |

# 1. Introduction

## 1.1 Overview

NRM1 is M.2 Module for application, such as M2M application and industrial IoT device platform based on 5G mmWave and sub-6/4G/3G networks for data communication.

## 1.2 Frequency Band and CA combinations

### 1.2.1 Frequency Bands

The operating frequencies in 5G, LTE and WCDMA modes conform to the 3GPP specifications.

**5G NR Sub6 Band supportive**

| NR Band | Duplex Mode | Uplink Frequency(MHz) | Downlink Frequency(MHz) | Channels | SCS (kHz) |
|---|---|---|---|---|---|
| **n1 -2100** | FDD | 1920 – 1980 | 2110 – 2170 | Tx: 384000 – 396000<br>Rx: 422000 - 434000 | 15 |
| **n2 – 1900 PCS** | FDD | 1850 – 1910 | 1930 – 1990 | Tx: 370000 – 382000<br>Rx: 386000 – 398000 | 15 |
| **n3 – 1800** | FDD | 1710 – 1785 | 1805 – 1880 | Tx: 342000 – 357000<br>Rx: 361000 – 376000 | 15 |
| **n5 – 850** | FDD | 824 – 849 | 869 – 894 | Tx: 164800 – 169800<br>Rx: 173800 – 178800 | 15 |
| **n7 – 2600** | FDD | 2500 – 2570 | 2620 - 2690 | Tx: 500000 – 514000<br>Rx: 524000 – 538000 | 15 |
| **n8 – 900** | FDD | 880 - 915 | 925 – 960 | Tx: 176000 – 183000<br>Rx: 185000 – 192000 | 15 |
| **N12 – 700a** | FDD | 699 - 716 | 729 - 746 | Tx: 139800 - 143200<br>Rx: 145800 - 149200 | 15 |

| | | | | | |
|---|---|---|---|---|---|
| **N20 – 800** | FDD | 832 - 862 | 791 - 821 | Tx: 166400 - 172400<br>Rx: 158200 - 164200 | 15 |
| **n25 -1900+** | FDD | 1850 - 1915 | 1930 - 1995 | Tx: 370000 - 383000<br>Rx: 386000 - 399000 | 15 |
| **n28 - 700 APT** | FDD | 703 - 748 | 758 - 803 | Tx: 140600 - 149600<br>Rx: 151600 - 160600 | 15 |
| **n38 - 2600** | TDD | 2570 - 2620 | | T/Rx: 514000 - 524000 | 30 |
| **n40 - 2300** | TDD | 2300 - 2400 | | T/Rx: 460000 - 480000 | 30 |
| **n41 - 2600+** | TDD | 2496 - 2690 | | T/Rx: 499200 - 537996 | 30 |
| **n48 - 3600** | TDD | 3550 - 3700 | | T/Rx: 636668 - 646666 | 30 |
| **n66 - AWS-4** | FDD | 1710 - 1800 | 2110 - 2200 | Tx: 342000 - 356000<br>Rx: 422000 - 440000 | 15 |
| **n71 - 600** | FDD | 663 - 698 | 617 - 652 | Tx: 132600 - 139600<br>Rx: 123400 - 130400 | 15 |
| **n77 - 3700** | TDD | 3300 - 4200 | | T/Rx: 620000 - 680000 | 30 |
| **n78 – 3500** | TDD | 3300 - 3800 | | T/Rx: 620000 - 653332 | 30 |
| **n79 - 4500** | TDD | 4400 - 5000 | | T/Rx: 693334 - 733332 | 30 |

5G NR mmWave Band supportive

| NR Band | Duplex Mode | Uplink Frequency (MHz) | Downlink Frequency (MHz) | Channels | SCS (kHz) |
|---|---|---|---|---|---|
| **n257- 28 GHz** | TDD | 26500 - 29500 | | T/Rx: 2054167 - 2104168 | 120 |
| **n258 - 26 GHz** | TDD | 24250 - 27500 | | T/Rx: 2016667 - 2070831 | 120 |
| **n260 - 39 GHz** | TDD | 37000 - 40000 | | T/Rx: 2229167 - 2279165 | 120 |
| **n261- 28 GHz US** | TDD | 27500 - 28350 | | T/Rx: 2070833 - 2084999 | 120 |

LTE Bands supportive

| E-UTRA Band | Duplex Mode | Uplink Frequency(MHz) | Downlink Frequency(MHz) | Channels |
|---|---|---|---|---|
| **B1 - 2100** | FDD | 1920 - 1980 | 2110 - 2170 | Tx: 18000 - 18599<br>Rx: 0 - 599 |
| **B2 - 1900 PCS** | FDD | 1850 - 1910 | 1930 - 1990 | Tx: 18600 – 19199 |

| | | | | |
|---|---|---|---|---|
| | | | | Rx: 600 - 1199 |
| **B3 - 1800+** | FDD | 1710 - 1785 | 1805 - 1880 | Tx: 19200 - 19949<br>Rx: 1200 - 1949 |
| **B4 - AWS-1** | FDD | 1710 - 1755 | 2110 - 2155 | Tx: 19950 - 20399<br>Rx: 1950 - 2399 |
| **B5 - 850** | FDD | 824 - 849 | 869 - 894 | Tx: 20400 - 20649<br>Rx: 2400 - 2649 |
| **B7 - 2600** | FDD | 2500 - 2570 | 2620 - 2690 | Tx: 20750 - 21449<br>Rx: 2750 - 3449 |
| **B8 - 900 GSM** | FDD | 880 - 915 | 925 - 960 | Tx: 21450 - 21799<br>Rx: 3450 - 3799 |
| **B12 - 700 a** | FDD | 699 - 716 | 729 - 746 | Tx : 23010 - 23179<br>Rx : 5010 - 5179 |
| **B13 - 700 c** | FDD | 777 - 787 | 746 - 756 | Tx : 27210 - 27659<br>Rx : 9210 - 9659 |
| **B14 - 700 PS** | FDD | 788 - 798 | 758 - 768 | Tx : 23280 - 23379<br>Rx : 5280 - 5379 |
| **B17 - 700 b** | FDD | 704 - 716 | 734 - 746 | Tx: 23730 - 23849<br>Rx: 5730 - 5849 |
| **B18 - 800 Lower** | FDD | 815 - 830 | 860 - 875 | Tx: 23850 - 23999<br>Rx: 5850 - 5999 |
| **B19 - 800 Upper** | FDD | 830 - 845 | 875 - 890 | Tx: 24000 - 24149<br>Rx: 6000 - 6149 |
| **B20 - 800 DD** | FDD | 832 - 862 | 791 - 821 | Tx: 24150 - 24449<br>Rx: 6150 - 6449 |
| **B25 - 1900+** | FDD | 1850 - 1915 | 1930 - 1995 | Tx: 8040 - 8689<br>Rx: 26040 - 26689 |
| **B26 - 850+** | FDD | 814 - 849 | 859 - 894 | Tx: 8690 - 9039<br>Rx: 26690 - 27039 |
| **B28 - 700 APT** | FDD | 703 - 748 | 758 - 803 | Tx: 9210 - 9659<br>Rx: 27210 - 27659 |
| **B29 - 700 d** | FDD | N/A | 717 - 728 | Rx: 9660 - 9769 |
| **B30 - 2300 WCS** | FDD | 2305 - 2315 | 2350 - 2360 | Tx: 9770 - 9869<br>Rx: 27660 - 27759 |

| | | | | |
|---|---|---|---|---|
| **B32 - 1500 L** | FDD | N/A | 1452 - 1496 | Rx: 9920 - 10359 |
| **B34 - 2000** | TDD | 2010 – 2025 | | T/Rx: 36200 - 36349 |
| **B38 - 2600** | TDD | 2570 - 2620 | | T/Rx: 37750 - 38250 |
| **B39 - 1900+** | TDD | 1880 - 1920 | | T/Rx: 38250 - 38649 |
| **B40 - 2300** | TDD | 2300 - 2400 | | T/Rx: 38650 - 39650 |
| **B41 - 2600+** | TDD | 2496 - 2690 | | T/Rx: 39650 - 41589 |
| **B42 - 3500** | TDD | 3400 - 3600 | | T/Rx: 41590 - 43589 |
| **B46 - 5200** | TDD | 5150 – 5925 (DL only) | | Rx: 46790 - 54539 |
| **B48 - 3600** | TDD | 3550 - 3700 | | T/Rx: 55240 - 56739 |
| **B66 - AWS-3** | FDD | 1710 - 1780 | 2110 - 2200 | Tx: 66436 - 67335<br>Rx: 131972 - 132671 |
| **B71 - 600** | FDD | 663 - 698 | 617 - 652 | Tx: 133122 - 133471<br>Rx: 68586 - 68935 |

### 1.2.2 Carrie Aggregation combinations(TBD)

There are 2CC, 3CC, 4CC and 5CC configurations shown in inter-band, and intra-band CA types in single duplex (FDD only) and in hybrid duplex (FDD+TDD) modes.

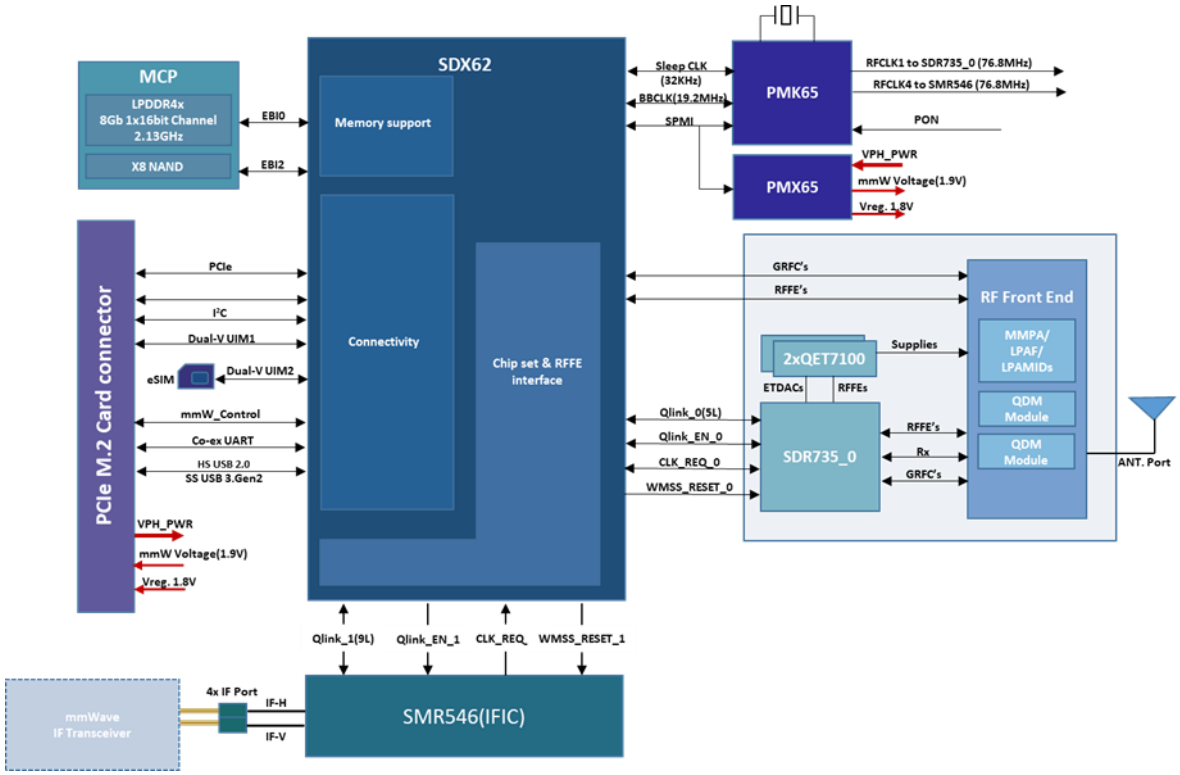
# 2. Main Features

## 2.1 Main Features

| Function | Features |
|---|---|
| **Physical** | M.2 Type 3253-XX-B |
| **Cellular technology** | 5G: FR1(Sub 6G), optional FR2(mmWave), Rel 15<br>4G: CAT. 20 (2Gbps) on DL, CAT. 13 (150Mbps) on UL, Rel 14<br>3G: HSPA+ Rel8 up to 42/11Mbps in DL/UL |
| **4x4 MIMO** | 5G: n1/2/3/66/7/41/77/78/79<br>4G: B1/25(2)/3/66(4)/7/30/40/41(38)/42/48 |
| **Diversity/2nd Rx** | 4G: all operating bands<br>3G: all operating bands |
| **GNSS** | Dual-Frequency GNSS<br>Upper L-band: GPS/Glonass/Beidou/Galileo<br>Lower L-band: GPS/Galileo |
| **USIM port – dual voltage** | Support for SIM<br>Class B and Class C support<br>Clock rates up to 4 MHz |
| **Application processor** | Application processor to run customer application code<br>32 bit ARM Cortex-A7 up to 1.5 GHz running the Linux operating system<br>8Gbit NAND Flash + 8Gbit LPDDR4 MCP is supported |
| **Main Interfaces** | PCIe Gen3 x 1-lane<br>USB 3.1 Gen 2<br>Peripheral Ports – GPIOs<br>I2C |
| **Antenna connection** | 4 x MHF-4 type Cellular/GNSS antenna connectors<br>1 x MHF-4 type Dedicated GNSS antenna connector |

| | |
|---|---|
| | 8 x mmWave IF connectors(option) |
| **Form factor** | M.2 Form factor (32 * 53 * 3.55 mm), accommodating the multiple RF bands |
| **Environment and quality requirements** | *The device is designed and qualified by Woori-net to satisfy environmental and quality requirements.* |
| **Single supply module** | The module internally generates all its required internal supply voltages. |
| **Operating temperature** | Range -20°C to +60°C (conditions as defined in Section 2.8.1, Temperature Range) |

## 2.2 Block Diagram



# 3. PINS ALLOCATION

## 3.1 Pin Assignment

| | | | |
|---|---|---|---|
| 1 | CONFIG_3 | VPH_PWR | 2 |
| 3 | GND | VPH_PWR | 4 |
| 5 | GND | FULL_CARD_PWR_OFF_N | 6 |
| 7 | NRM1_USB_HS_DP | M2_W_DISABLE1_3P3_N_CONN | 8 |
| 9 | NRM1_USB_HS_DM | LED1(Hi-Z) | 10 |
| 11 | GND | | |
| | Module Key | Module Key | |
| 21 | CONFIG_0/GND | GPIO_5(QTM545 Thermistor) | 20 |
| 23 | RCED_USB_BOOT/MDM_GPIO_42 | GPIO_6(QTM545 Thermistor) | 22 |
| 25 | SDM_GRFC_77 | GPIO_7(QTM545 Thermistor) | 24 |
| 27 | GND | M2_W_DISABLE2_3P3_N_CONN | 26 |
| 29 | USB3.0_SS_TX_M | GPIO_8(QTM545 Thermistor) | 28 |
| 31 | USB3.0_SS_TX_P | UIM1_RST | 30 |
| 33 | GND | UIM1_CLK | 32 |
| 35 | USB3.0_SS_RX_M | UIM1_DATA | 34 |
| 37 | USB3.0_SS_RX_P | VREG_L11_1P8(UIM_PWR) | 36 |
| 39 | GND | SDX65_GPIO_32_CONN | 38 |
| 41 | PCIE_HST_TX0_M | QTM0_PON | 40 |
| 43 | PCIE_HST_TX0_P | QTM1_PON | 42 |
| 45 | GND | QTM2_PON | 44 |
| 47 | PCIE_HST_RX0_M | QTM3_PON | 46 |
| 49 | PCIE_HST_RX0_P | VREG_S4_1P9 | 48 |
| 51 | GND | GPIO_57/PCIE_RST_N | 50 |
| 53 | PCIE_HST_REFCLK_M | GPIO_56/PCIE_CLK_REQ_N | 52 |
| 55 | PCIE_HST_REFCLK_P | GPIO_53/PCIE_WAKE_N | 54 |
| 57 | GND | I2C_SDA | 56 |
| 59 | GPIO_102 | I2C_SCL | 58 |
| 61 | GPIO_36/RFFE0_DATA | GPIO_103(interrupt) | 60 |
| 63 | GPIO_37/RFFE0_CLK | GPIO_45/WLAN_LTE_COXM_RXD | 62 |
| 65 | VREG_L6_1P8 | GPIO_44/WLAN_LTE_COXM_TXD | 64 |
| 67 | NR_RESIN_N | UIM1_PRESENT(internal 100K pull-up with 1.8V) | 66 |
| 69 | CONFIG_1/GND | GPIO_65 | 68 |
| 71 | GND | VPH_PWR | 70 |
| 73 | GND | VPH_PWR | 72 |
| 75 | CONFIG_2/GND | VPH_PWR | 74 |

## 3.2 I/O Parameter definitions

I/O Parameters Definition

| Type | Description |
|---|---|
| **AI** | Analog Input |
| **AO** | Analog Output |
| **DI** | Digital Input |
| **DO** | Digital Output |
| **IO** | Bidirectional |
| **OD** | Open Drain |
| **PI** | Power Input |
| **PO** | Power Output |

## 3.3 Pin Description

| Pin | Signal | I/O | Function | Type |
|---|---|---|---|---|
| **Power(5 pins) and Ground(11 pins)** | | | | |
| **2,4,70,72,74** | VPH_PWR | I | Power supply(+3.3V source) | 3.3V Power |
| **3,5,11,27,33,39,45,51,57,71,73** | GND | | Return current path | 0V |

| Pin | Signal | I/O | Function | Type |
|---|---|---|---|---|
| **USB Communication Port** | | | | |
| **7** | USB_HS_DP | I/O | USB 2.0 Data Plus | Analog |
| **9** | USB_HS_DM | I/O | USB 2.0 Data Minus | Analog |
| **29** | USB_SS_TX_M | O | USB 3.0 super-speed transmit-Minus | Analog |
| **31** | USB_SS_TX_P | O | USB 3.0 super-speed transmit-Plus | Analog |
| **35** | USB_SS_RX_M | I | USB 3.0 super-speed receive-Minus | Analog |
| **37** | USB_SS_RX_P | I | USB 3.0 super-speed receive-Plus | Analog |

| | | | | |
|---|---|---|---|---|
| **PCIe Communication Port** | | | | |
| **43** | PCIE_TX0_P | O | PCIe transmit 0 –plus | Analog |
| **41** | PCIE_TX0_M | O | PCIe transmit 0 –minus | Analog |
| **49** | PCIE_RX0_P | I | PCIe receive 0 –plus | Analog |
| **47** | PCIE_RX0_M | I | PCIe receive 0 –minus | Analog |
| **55** | PCIE_REFCLK_P | I | PCI Express differential reference clock – plus | Analog |
| **53** | PCIE_REFCLK_M | I | PCI Express differential reference clock – minus | Analog |
| **52** | PCIE_CLKREQ_N | I/O | PCIE reference clock request signal | 3.3V |
| **50** | PCIE_RESET_N | I/O | Functional reset to the PCIe bus | 3.3V |
| **54** | PCIE_WAKE_N | I/O | PCIe wake-up | 3.3V |
| **SIM Card Interface** | | | | |
| **36** | UIM_VCC | O | Supply output for an external UIM1 card | 1.8V /2.85V Power |
| **34** | UIM1_DATA | I/O | Data connection with an external UIM1 card | 1.8V /2.85V |
| **32** | UIM1_CLK | O | Clock output to an external UIM1 card | 1.8V /2.85V |
| **30** | UIM1_RESET_N | O | Reset output to an external UIM1 card | 1.8V /2.85V |
| **66** | UIM1_PRESENT | I | UIM1 Card Present Detect (internal 100K pull-up with 1.8V) | 1.8V |
| **Turn On/Off** | | | | |
| **6** | FULL_CARD_PWR_OFF_N | I | Module On/Off | 1.8V/3.3V |
| **67** | RESIN_N | I | Module reset | 1.8V |
| **Status indication** | | | | |
| **10** | LED | I | LED Control | Open Drain |
| **I2C Interface** | | | | |
| **56** | I2C_SDA | I/O | I2C Data | 1.8V |
| **58** | I2C_SCL | I/O | I2C Clock | 1.8V |
| **WLAN Control Interface** | | | | |
| **64** | COEX_UART_TX | I/O | WLAN/WWAN transmitter sync for coexistence with UART | 1.8V |

| | | | | |
|---|---|---|---|---|
| **62** | COEX_UART_RX | I/O | WLAN/WWAN receiver sync for coexistence with UART | 1.8V |
| **Antenna Control Interface** | | | | |
| **40** | QTM0_PON | O | External mmWave module control signal | 1.8V |
| **42** | QTM1_PON | O | External mmWave module control signal | 1.8V |
| **44** | QTM2_PON | O | External mmWave module control signal | 1.8V |
| **46** | QTM3_PON | O | External mmWave module control signal | 1.8V |
| **61** | RFFE0_CLK | I/O | RF front end interface clock | 1.8V |
| **63** | RFFE0_DATA | I/O | RF front end interface data | 1.8V |
| **ADC Interface** | | | | |
| **20** | GPIO_5 | AI | General purpose analog to digital converter interface | |
| **22** | GPIO_6 | AI | General purpose analog to digital converter interface | |
| **24** | GPIO_7 | AI | General purpose analog to digital converter interface | |
| **28** | GPIO_8 | AI | General purpose analog to digital converter interface | |
| **GPIO Interface** | | | | |
| **38** | GPIO_32 | I/O | General GPIO | 1.8V<br>Interrupt GPIO |
| **59** | GPIO_102 | I/O | General GPIO | 1.8V |
| **60** | GPIO_103 | I/O | General GPIO | 1.8V<br>Interrupt GPIO |
| **68** | GPIO_65 | I/O | General GPIO | 1.8V<br>Interrupt GPIO |
| **Other Pins** | | | | |
| **23** | FORCED_USB_BOOT | I | Forced USB boot | 1.8V |
| **8** | W_DISABLE1_3P3_N | I | Disable radio operation | 3.3V |
| **26** | W_DISABLE2_3P3_N | I | Disable radio operation | 3.3V |

| | | | | |
|---|---|---|---|---|
| ***25*** | *GRFC_77/GPIO_77* | *I/O* | *Generic RF controller bit* | *1.8V* |
| **48** | VREG_S4_1P9 | O | SMPS switch voltage | 1.9V Power |
| **65** | VREG_L6_1P8 | O | Reference Voltage | 1.8V Power |

## 3.4 Signal that Must be connected

Below table specifies the signals that must be connected for a debugging purpose even if not used by the end application.

Mandatory Signals

| Pin | Signal | Note |
|---|---|---|
| **2,4,70,72,74** | VBATT | |
| **3,5,11,27,33,39,45,51,57,71,73** | GND | |
| **7** | USB_HS_DP | |
| **9** | USB_HS_DM | |
| **23** | FORCED_USB_BOOT | |

## 3.5 Configuration Pins

| State# | Module Configuration Decodes | | | | Module Type and Main Host Interface |
|---|---|---|---|---|---|
| | CONFIG_0 (Pin 21) | CONFIG_1 (Pin 69) | CONFIG_2 (Pin 75) | CONFIG_3 (Pin 1) | |
| **0** | GND | N/C | N/C | N/C | WWAN-PCIe |
| **1** | N/C | N/C | N/C | GND | WWAN-USB3.0 |

# 4. RF Specification

## 4.1 RF performance

The RF performance in 5G, LTE and WCDMA modes conform to the 3GPP specifications

### 4.1.1 Maximun Transmit Output Power

TX power follows the measurement conditions and specifications defined in 3GPP.

| Band | Power class |
|---|---|
| **5G NR Sub-6** | 3 (0.2W) |
| **5G NR sub-6 Bands n41, n77, n78, n79 Supports Power Class 2** | TBD |
| **5G NR mmWave (OTA)** | 3 (0.2W) |
| **LTE All Bands** | 3 (0.2W) |
| **LTE Band 41 Supports Power Class 2** | 3 (0.2W) |

### 4.1.2 Minimum Receiver Sensitivity

Receiver Sensitivity follows the measurement conditions and specifications defined in 3GPP.

| Technology | 3GPP Compliance |
|---|---|
| **5G NR Sub-6** | Throughput >95% |
| **5G NR mmWave** | Throughput >95% |
| **4G LTE** | Throughput >95% |

| E-UTRA Band | Typical Rx Sensitivity (dBm) (BW=10MHz/ B46 BW=20mHz) | | | | |
|---|---|---|---|---|---|
| **Antenna Configuration** | **PRx** | **DRx** | **MIMO 0** | **MINO 1** | **Combined** |
| **LTE FDD B1** | -97 | -98 | -97 | -97 | -103 |

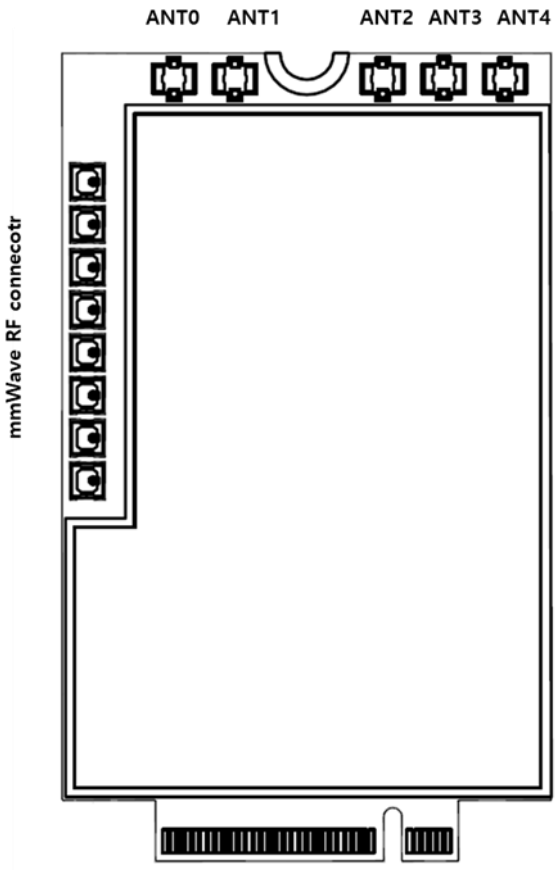
| | | | | | |
|---|---|---|---|---|---|
| **LTE FDD B2** | -97 | -97 | -97 | -97 | -103 |
| **LTE FDD B3** | -97 | -98 | -97 | -97 | -103 |
| **LTE FDD B4** | -97 | -98 | -97 | -97 | -103 |
| **LTE FDD B5** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B7** | -96 | -97 | -97 | -97 | -102 |
| **LTE FDD B8** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B12** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B13** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B14** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B17** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B18** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B19** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B20** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B25** | -97 | -97 | -97 | -97 | -103 |
| **LTE FDD B26** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B28** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B29(DL only)** | -99 | -99 | NA | NA | -102 |
| **LTE FDD B30** | -96 | -98 | -97 | -97 | -102 |
| **LTE FDD B32** | -97 | -98 | -97 | -97 | -102 |
| **LTE TDD B34** | -97 | -98 | TBD | TBD | TBD |
| **LTE TDD B38** | -97 | -97 | -96 | -96 | -102 |
| **LTE TDD B39** | -97 | -98 | -97 | -97 | -103 |
| **LTE TDD B40** | -96 | -98 | -96 | -96 | -102 |
| **LTE TDD B42** | -96 | -97 | -96 | -96 | -102 |
| **LTE TDD B46(DL only)** | -93 | -92 | -92 | -93 | -98 |
| **LTE TDD B48** | -96 | -97 | -96 | -97 | -102 |
| **LTE FDD B66** | -97 | -97 | -97 | -97 | -103 |

| | | | | | |
|---|---|---|---|---|---|
| **LTE FDD B71** | -99 | -99 | NA | NA | -102 |

*3.3Voltage/ Room temperature

## 4.2 Antenna specification

### 4.2.1 Antenna Configuration



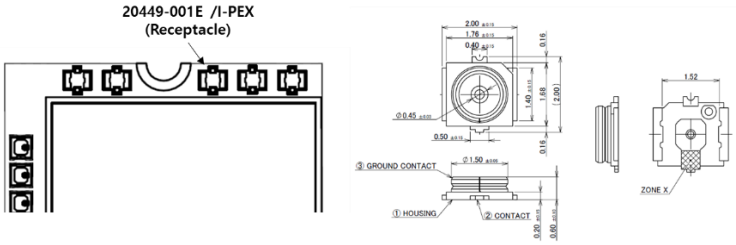
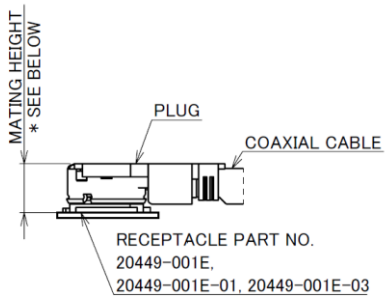

Refer to the following antenna configuration assigned.

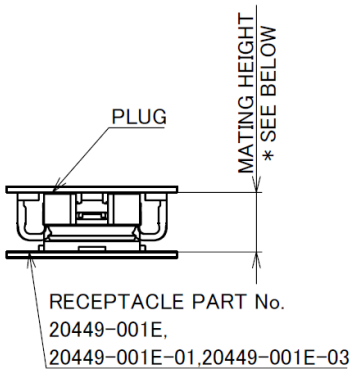
| Antenna Port | Technology | Tx | Rx | GNSS |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| **ANT0** | **LTE** | B1, B2, B3, B4, B5, B7,B8, B12, B13, B14,B17, B18, B19, B20,B25, B26, B28, B30,B34, B38, B39, B40,B41, B66, B71 | B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B29,B30, B32, B34, B38, B39, B40, B41, B42,B46, B48, B66, B71 | - |
| | **5G NR FR1** | n1, n2, n3, n5, n7, n8, n12, n20, n28, n38, n40, n41, n66, n71 | n1, n2, n3, n5, n7, n8, n12, n20, n25, n28, n38, n40, n41, n48, n66, n71, n77, n78, n79 | - |
| **ANT1** | **LTE** | B1, B2, B3, B4, B7,B25, B41, B66 | B1, B2, B3, B4, B7, B25, B30, B32, B34, B38, B39, B40, B41, B42, B46, B48, B66 | - |
| | **5G NR FR1** | n1, n2, n3, n5, n7, n25, n41, n66 | n1, n2, n3, n7, n25, n38, n40, n41, n48, n66, n77, n78, n79 | - |
| **ANT2** | **LTE** | B5, B20, B42, B48, B71 | B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B18, B19, B20, B25, B26, B28, B29, B30, B32, B34, B38, B39, B40, B41, B42, B46, B48, B66, B71 | - |
| | **5G NR FR1** | n48, n71, n77, n78, n79 | n1, n2, n3, n5, n7, n8, n12, n20, n25, n28, n38, n40, n41, n48, n66, n71, n77, n78, n79 | - |
| **ANT3** | **LTE** | - | B1, B2, B3, B4, B7, B25, B30, B32, B34, B38, B39, | - |

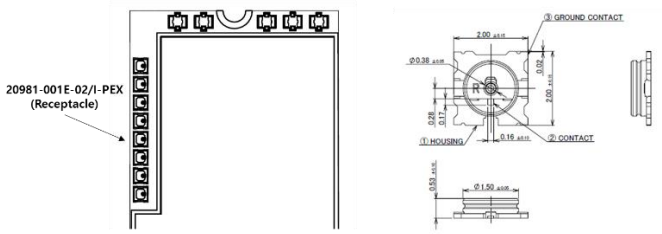
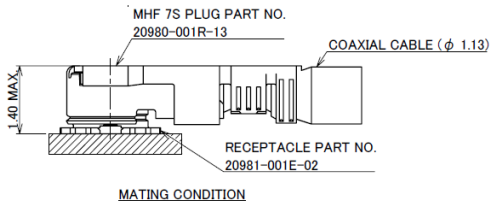
| | | | | |
|---|---|---|---|---|
| | | | B40, B41, B42, B46, B48, B66 | |
| | **5G NR FR1** | - | n1, n2, n3, n7, n25, n38, n40, n41, n48, n66, n77, n78, n79 | GPS L1, Galileo E1, Beidou B1, Glonass G1 |
| **ANT4** | **GNSS** | - | - | GPS L1, Galileo E1, Beidou B1, Glonass G1 |

4.2.2 Antenna Connector

| **RECEPTACLE** | | |
|---|---|---|
|  | | **Receptacle Part No.(I-PEX)**<br>20449-001E<br>20449-001E-01<br>20449-001E-03 |
| **PLUG** | | |
| **COAXIAL CABLE Type** |  | **Cable type plug Part No. (I-PEX)**<br>**Mating height**<br>**Max.1.2T**<br>20611-001R<br>20572-001R-8,<br>20448-00*R-081<br>20448-001R-081E<br>**Max.1.4T**<br>20565-001R-** |

| | | |
|---|---|---|
| | | **Max.1.7T**<br>20632-001R-37 |
| **SMT**<br>**Type** |  | **SMT type plug Part No. (I-PEX)**<br>**Mating height**<br>**Max.1.2T**<br>20462-001E (I-PEX) |

4.2.3 mmWave Antenna Connector

| **RECEPTACLE** | |
|---|---|
|  | **MHF 7S Receptacle Part No.**<br>20981-001E-02 (I-PEX) |
| **PLUG** | |
|  | **MHF 7S PLUG Part No.**<br>**Max.1.4T**<br>20980-001R-13 (I-PEX) |

4.2.4 Antenna Requirements

The antenna must specifications meet the following requirements

LTE/5G Sub-6 Antenna Requirements

| | |
|---|---|
| **Frequency Range** | Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s) |
| **Impedance** | 50Ω |
| **Input Power** | > 24 dBm average power in LTE & 5G Sub-6 |
| **VSWR absolute max.** | <= 10:1 |
| **VSWR recommended** | <= 2:1 |

### 4.2.5 GNSS Receiver

The NRM1 integrates a GNSS receiver that could be used in Standalone mode and in A-GPS (assisted GPS), according to the different configurations.

| | |
|---|---|
| **Frequency Range** | • Wide-band GNSS: 1559–1606 MHz recommended<br>• GPS: 2.046 MHz BW NB GPS (centered on 1575.42 MHz)<br>• Glonass (GLO): ~ 8.3 MHz BW (1597–1606 MHz)<br>• BeiDou (BDS): 4.092 MHz BW (1559.05 – 1563.14 MHz)<br>• Galileo (GAL): 4.092 MHz BW (centered on 1575.42 MHz) |
| **Impedance** | 50Ω |
| **Gain** | 1.5 dBi < Gain < 3 dBi |
| **Amplification** | 18 dB < Gain < 21 dB |
| **Supply Voltage** | 3.1 V |
| **Current consumption** | 20 mA Typical |

#### 4.2.6 GNSS RF Front End Design(TBD)

*The NRM1 contains an integrated LNA and pre-select SAW filter. This allows the module to work well with a passive GNSS antenna. If the antenna cannot be located near the NRM1, then an active antenna (that is, an antenna with a low noise amplifier built in) can be used with an external dedicated power supply circuit. GNSS receive path uses either the dedicated GNSS connector or the shared Secondary #0 antenna connector.*

# 5. Application Interface

## 5.1 Power Sources

#### 5.1.1 Power Supply Requirements

| | |
|---|---|
| **Nominal supply voltage** | 3.3V |
| **Supply voltage range** | 3.135V – 3.465V |
| **Maximum ripple on module input supply** | 30 mV |
| **Peak current consumption without mmWave antenna module** | 3.3V @ 4 A |

#### 5.1.2 Power Consumption(TBD)

Below table provides typical current consumption values of NRM1 for various operation modes.

Current Consumption

| Mode | Average[Typ.] | Mode Description |
|---|---|---|

| | | |
|---|---|---|
| **IDLE Mode** | | |
| **CFUN=1** | TBD | No call connection<br>USB2.0 is connected to a host |
| **Power Saving Mode (PSMWDISACFG=1, W_DISABLE_N:Low)** | | |
| **CFUN=4** | | Tx and Rx are disabled; module is not registered on the network (Flight mode) |
| **CFUN=5** | | in standby mode |
| **Operative Mode (LTE)** | | |
| **Single mode (1DL/1UL SISO)** | 800mA | Non-CA ,B2 BW 5MHz, 1 RB, 23dBm, QPSK DL / QPSK UL |
| **2DLCA(4x4MIMO) with 2ULCA(SISO)** | 1300mA | CA_2A-66A, BW 20MHz, Full RB, 256QAM DL / 256QAM UL(800Mbps DL / 170Mbps UL) |
| **7DLCA(2x2MIMO) with 1UL(SISO)** | 1500mA | CA_2A-13A-46D-66A-66A, Full RB, 256QAM DL/ 64QAM UL(1300Mbps DL / 75Mbps UL) |
| **5DLCA (4x4MIMO) With 1UL(SISO)** | 1900mA | CA_1A-3C-7C, Full RB, 256QAM DL/ 64QAM UL(2Gbps DL / 75Mbps UL) |
| **Operative Mode (NR-FR1)** | | |
| **NSA mode 1CC+1FR1** | 1000mA | EN-DC_1A(1DL/UL SISO)-n78A(1DL/1UL SISO)<br>LTE : BW 20MHz, 1 RB, QPSK DL / QPSK UL, 23dBm<br>FR1 : BW 100MHz, Inner RB 137(Number)@64(Position), QPSK DL / QPSK UL, 23 dBm |
| **NSA mode 5CC+1FR1** | 2300mA | EN-DC_1A-3C-7C(5DL 4x4MIMO/1UL SISO)- n78(1DL 4x4MIMO/1UL SISO)<br>LTE : BW 20MHz, Full RB, 256QAM DL / 64QAM UL(2Gbps DL / 75Mbps UL)<br>FR1 : BW100MHz, Full RB, 256QAM DL /256QAM UL(1.6Gbps DL/118Mbps) |

| Operative Mode (NR-FR2) | | |
|---|---|---|
| **TBD** | TBD | TBD |

*3.3V / room temperature

## 5.2 Operating Modes(TBD)

| Mode | Details | |
|---|---|---|
| **Normal Operation mode** | *Idle* | *Software is active. The module has registered on the network, and it is ready to send and receive data.* |
| | *Talk/Data* | *Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.* |
| **Minimum Functionality Mode** | ***AT+CFUN=0*** *command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.* | |
| **Airplane Mode** | ***AT+CFUN=4*** *command or driving W_DISABLE# low can set the module to airplane mode. In this case, RF function will be invalid.* | |
| **Sleep Mode** | *In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.* | |
| **Power Down Mode** | In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. | |

## 5.3 Turn on and off Scenarios

### 5.3.1 Full_CARD_PWR_OFF_N

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **Turn On/Off** | | | | |
| **6** | FULL_CARD_PWR_OFF_N | I | Module On/Off | 1.8V/3.3V |

FULL_CARD_POWER_OFF# signal is an Active Low input that is used to turn off the entire module. When the input signal is asserted high (≥1.19 V) the Module will be enabled. When the input signal is driven low signal (≤0.2 V), it will force the module to shut down.
The FULL_CARD_POWER_OFF# pin has internally pulled low with a weak pull-down 100 kΩ resistor. The input must be 3.3 V tolerant but can be driven by either 1.8 V or 3.3 V GPIO.

### 5.3.2 Power On/Off

To turn on the device, the FULL_CARD_POWER_OFF_N pin must be asserted high.

Power off the device can be done in three different ways:

- *Graceful Shutdown by FULL_CARD_POWER_OFF_N or AT command AT#SHDN*
- *Fast Shutdown by GPIO triggered or AT command AT#FASTSHDN*
- *Unconditional Shutdown using the SYS_RESIN_N*

## 5.4 Reset the Module

Device reset can be achieved as follows:

- *Graceful Reset by USB AT command AT#REBOOT*
- *Unconditional Reset using the SYS_RESIN_N*

### 5.4.1 Graceful Reset

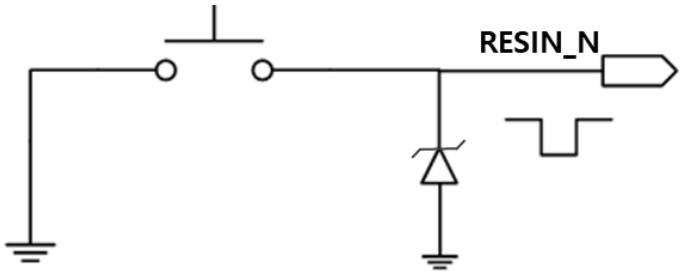
To gracefully restart the module, AT#REBOOT AT command must be sent.

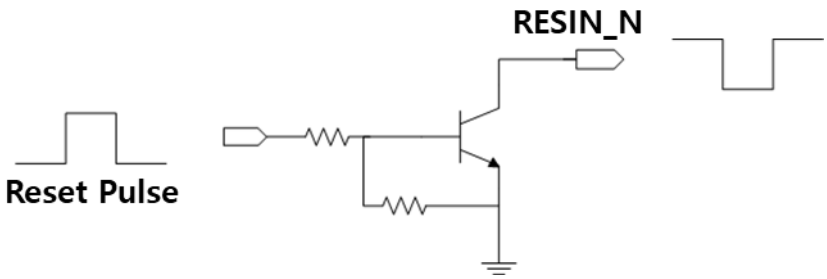
### 5.4.2 Hardware Reset

Asynchronous RESIN_N pin, active low. Whenever this pin is active, the modem will immediately be placed in a Power On reset condition. Care should be taken not to activate this pin unless there is a critical failure and all other methods of regaining control and/or communication with the WWAN sub-system have failed.

| Pin Name | Pin No. | Description | DC Characteristics |
|---|---|---|---|
| **RESIN_N** | 67 | Reset the module | $V_{IHmin}$=1.2V<br>$V_{ILMAX}$=0.6V |

A Button or open drain/collector driver can be used to control the RESIN_N.

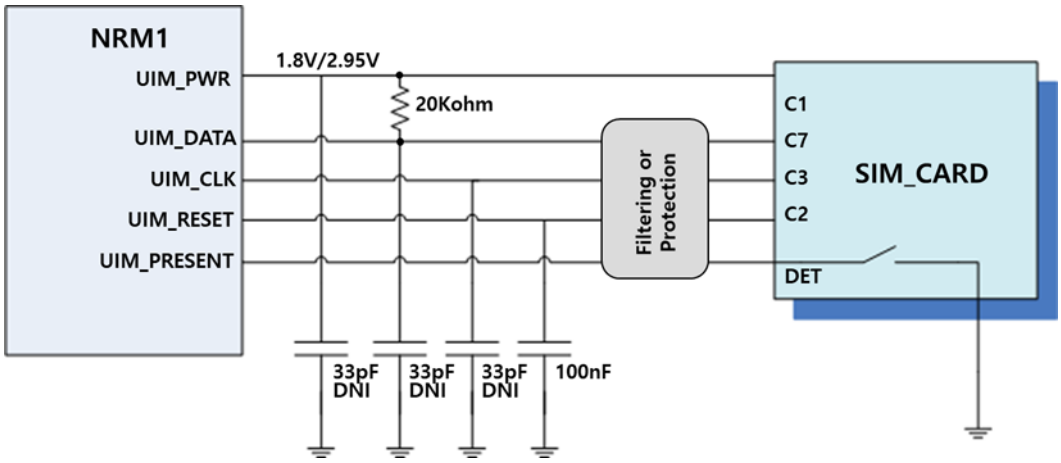


## 5.5 (U)SIM Interface

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **USB Communication Port** | | | | |
| **36** | UIM_VCC | O | Supply output for an external UIM1 card | |
| **34** | UIM1_DATA | I/O | Data connection with an external UIM1 card | |
| **32** | UIM1_CLK | O | Clock output to an external UIM1 card | |
| **30** | UIM1_RESET_N | O | Reset output to an external UIM1 card | |
| **66** | UIM1_PRESENT | I | UIM1 Card Present Detect (internal 100K pull-up with 1.8V) | |

NRM1 provides one (U)SIM interface and eSIM. (U)SIM is dual-voltage 1.8V or 2.85V interface. There is an embedded SIM on NRM1. If you want to use the eSIM which is mounted on NRM1, please contact Woori-net.




✓ UIM_PRESENT pin has internal 100Kohm pull-up on the module tied to its 1.8V power rail.

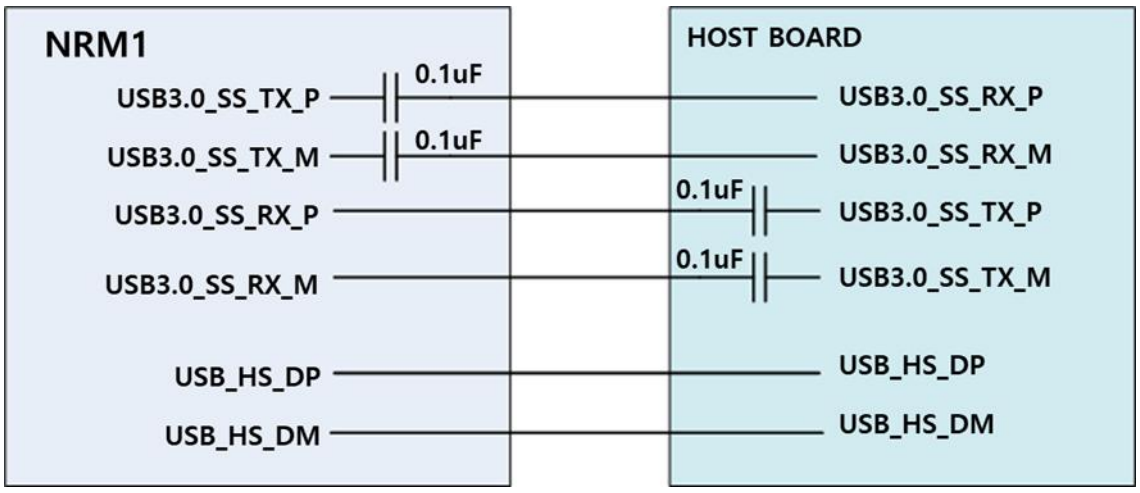
✓ (U)SIM Layout guidelines

- Ensure that the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector

## 5.6 USB Interface

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **USB Communication Port** | | | | |
| **7** | USB_HS_DP | I/O | USB 2.0 Data Plus | Must be connected |
| **9** | USB_HS_DM | I/O | USB 2.0 Data Minus | |
| **29** | USB_SS_TX_M | O | USB 3.0 super-speed transmit-Minus | If unused, Keep it open. |
| **31** | USB_SS_TX_P | O | USB 3.0 super-speed transmit-Plus | If unused, Keep it open. |
| **35** | USB_SS_RX_M | I | USB 3.0 super-speed receive-Minus | If unused, Keep it open. |
| **37** | USB_SS_RX_P | I | USB 3.0 super-speed receive-Plus | If unused, Keep it open. |

The module includes super-speed USB3.1 Gen2 with high-speed USB2.0 backward compatibility. It is compliant with Universal Serial Bus Specification, Revision 3.0 and can be used for control and data transfers as well as for diagnostic monitoring and firmware update. USB 3.1 needs AC coupling series capacitors on the TX lines in both directions. In order to interface USB3.1 with the application board controlling the modem, 0.1uF capacitors should be installed on USB_SS_RX_P/M lines of the module. Series capacitors are already placed on USB_SS_TX_P/M lines inside the Module.




- ✓ Require series capacitors on USB3.0_SS_RX_P/M.
- ✓ The series capacitors must be placed close to the host.
- ✓ USB Layout guidelines
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities.
- Keep isolation between the Tx pair, and DP/DM to avoid crosstalk.
- If core vias are used, use no more than two core vias per signal line to limit stubs.
- If the total length of USB 3.0 signal traces exceeds 50 mm, route the lines with a zigzag pattern greater than 10° to avoid ER mismatch caused by the glass-weave effect.
- The impedance of USB differential trace is 90 Ω.

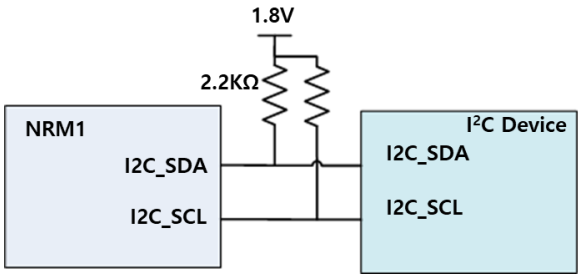
## 5.7 I²C Interface

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **I2C Interface** | | | | |
| **56** | I2C_SDA | I/O | I2C Data | If unused, Keep it open. |
| **58** | I2C_SCL | I/O | I2C Clock | If unused, Keep it open. |

The I2C interface is used for controlling peripherals inside the module.

If I2C interface are used, 2.2K Ω pull-up registers are required in the customer board

If not used as I2C, it can be used as general GPIO.



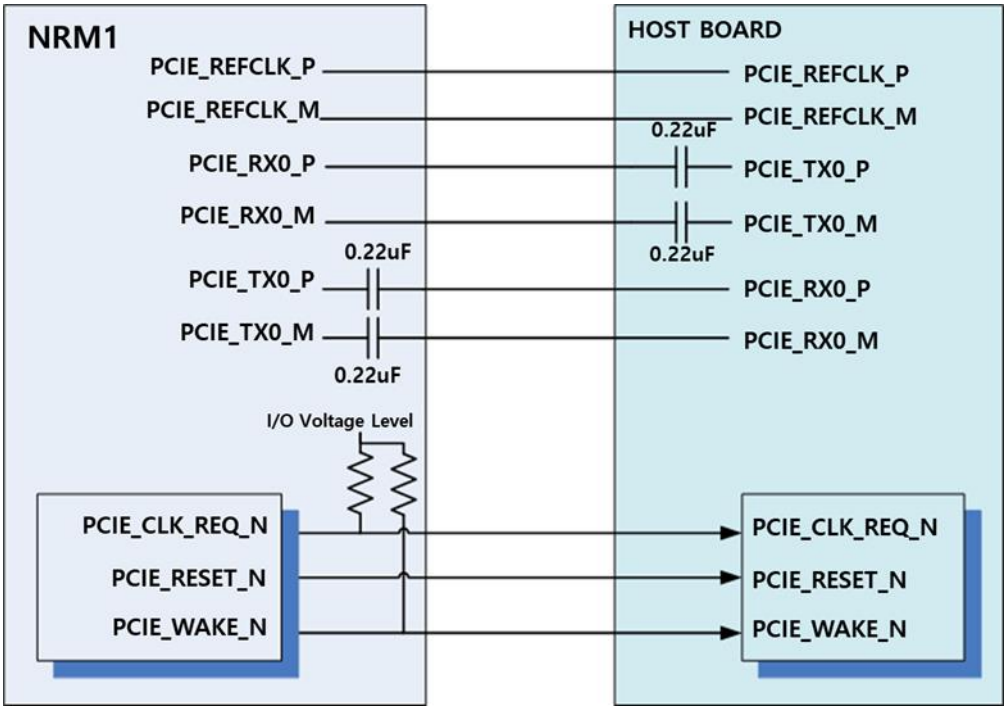

✓ $I^2C$ Layout guidelines

- When routing these traces, it is important to avoid routing of any aggressor traces in an adjacent layer

## 5.8 PCIe Interface

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **PCIe Communication Port** | | | | |
| **43** | PCIE_TX0_P | O | PCIe transmit 0 –plus | If unused, Keep it open. |
| **41** | PCIE_TX0_M | O | PCIe transmit 0 –minus | If unused, Keep it open. |
| **49** | PCIE_RX0_P | I | PCIe receive 0 –plus | If unused, Keep it open. |
| **47** | PCIE_RX0_M | I | PCIe receive 0 –minus | If unused, Keep it open. |
| **55** | PCIE_REFCLK_P | I | PCI Express differential reference clock – plus | If unused, Keep it open. |
| **53** | PCIE_REFCLK_M | I | PCI Express differential reference clock – minus | If unused, Keep it open. |
| **52** | PCIE_CLKREQ_N | I/O | PCIE reference clock request signal | If unused, Keep it open. |
| **50** | PCIE_RESET_N | I/O | Functional reset to the PCIe bus | If unused, Keep it open. |
| **54** | PCIE_WAKE_N | I/O | PCIe wake-up | If unused, Keep it open. |

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface which complies with the PCI Express Specification, Gen 3(Data rate is 4Gpbs) and Gen 4(16Gbps)*.




* Link speed described per supported PCIe Generation standard. Actual throughput at the system level could be lower due to overheads.

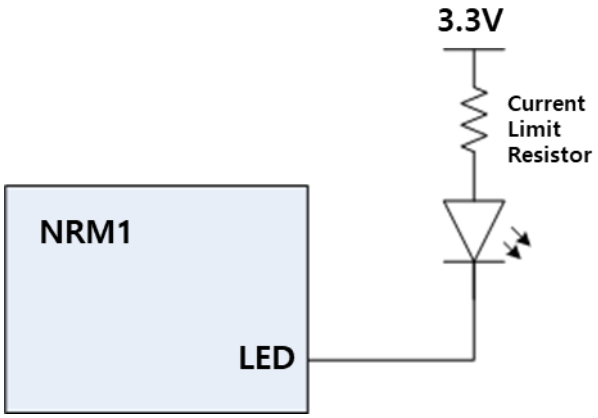
- ✓ Require series capacitors on PCIe_TX_P/M.
- ✓ The series capacitors must be placed close to the host.
- ✓ PCIe Layout guidelines
- Route differential pairs in the inner layers with a solid GND reference to have good impedance control and to minimize discontinuities. Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces.
- For PCIe signal traces, the maximum length of each differential data pair(TX/RX) is recommended to be less than 200mm, and each differential data pair matching should be less than 0.7mm(5ps)
- The impedance of PCIe differential trace is 90 Ω.

## 5.9 LED

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **Status indication** | | | | |
| **10** | LED | I | LED Control | If unused, Keep it open. |

The LED pin is set as the module status indicator.

The LED signal is provided to enable wireless communication add-in card to provide status indications to users via system provided indication. The LED output signals is active low and is intended to drive system-mounted LED indicators.




## 5.10 Antenna Tuner Control Interfaces

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **Antenna Control Interface** | | | | |
| **40** | QTM0_PON | O | External mmWave module control signal | If unused, keep it open. |
| **42** | QTM1_PON | O | External mmWave module control signal | If unused, keep it open. |

| | | | | |
|---|---|---|---|---|
| **44** | QTM2_PON | O | External mmWave module control signal | If unused, keep it open. |
| **46** | QTM3_PON | O | External mmWave module control signal | If unused, keep it open. |
| **61** | RFFE0_CLK | I/O | RF front end interface clock | If unused, keep it open. |
| **63** | RFFE0_DATA | I/O | RF front end interface data | If unused, keep it open. |

The module supports external antenna tuner control through either RFFE interface or dedicated GPIO interfaces. Customers can choose either one according to their tuner design.

## 5.11 ADC Interface

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **ADC Interface** | | | | |
| **20** | GPIO_5 | AI | General purpose analog to digital converter interface | If unused, keep it open. |
| **22** | GPIO_6 | AI | General purpose analog to digital converter interface | If unused, keep it open. |
| **24** | GPIO_7 | AI | General purpose analog to digital converter interface | If unused, keep it open. |
| **28** | GPIO_8 | AI | General purpose analog to digital converter interface | If unused, keep it open. |

**If usage scenario is provided, we will discuss how to use this pins.*

The module provides two Analog-to-Digital Converters (ADC) interfaces. ADC pins can read the voltage.

## 5.12 GPIO Interface

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **GPIO Interface** | | | | |
| **38** | GPIO_32 | I/O | General GPIO | If unused, keep it open. |
| **59** | GPIO_102 | I/O | General GPIO | If unused, keep it open. |
| **60** | GPIO_103 | I/O | General GPIO | If unused, keep it open. |
| **68** | GPIO_65 | I/O | General GPIO | If unused, keep it open. |
| **56** | I2C_SDA/GPIO_10 | I/O | General GPIO | If unused, Keep it open. |
| **58** | I2C_SCL/GPIO_11 | I/O | General GPIO | If unused, Keep it open. |

**If there is a shortage of GPIO pin, we will suggest other pins that can be used.*

The general-purpose I/O GPIO pin can be configured to act in input or output.
Input pins can only be read and report digital values(high or low) present on the pin the read time.
Output pins can only be set or the pin level can be queried

### 5.12.1 Using a GPIO pin as Input

GPIO pins, when used as inputs, can be tied to a digital output of another device and report its status, provided the device interface levels are compatible with the GPIO 1.8V CMOS levels. If a digital output of a device is tied to GPIO input, the pin has interface levels different than 1.8V CMOS. It can be buffered with an open collector transistor with a pull-up resistor to 1.8V. An interrupt GPIO pins allows the level or edge of the input signal, with selectable polarity, to generate an interrupt.

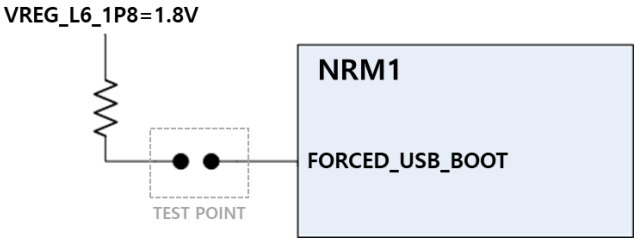
### 5.12.2 Using a GPIO Pin as output

GPIO pins, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pins have a push-pull output, and therefore the pull-up resistor can be omitted.

## 5.13 FORCED_USB_BOOT Interface

| Pin | Signal | I/O | Function | Comment |
|---|---|---|---|---|
| **FORCED_USB_BOOT** | | | | |
| **23** | FORCED_USB_BOOT | I | Forced USB boot | Must be connected to TP |

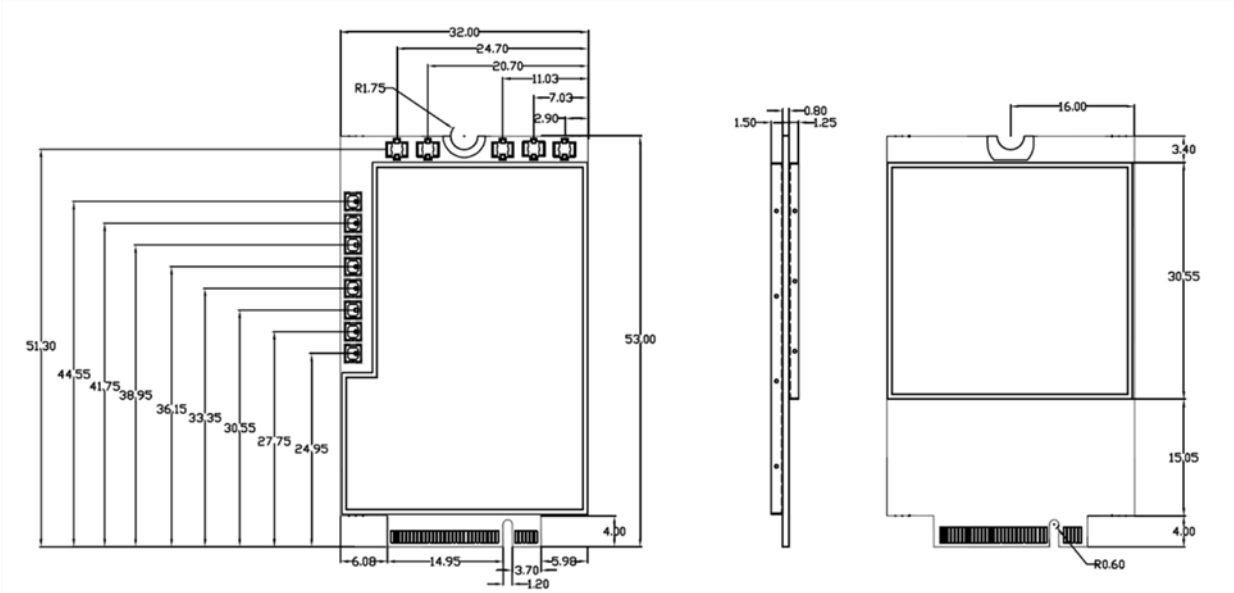
During development or factory production, a boot from the USB port can be forced by using Pin. FORECED_USB_BOOT. FORECED_USB_BOOT = 1 forces the SDX device to boot from the USB port.




# 6. Mechanical Dimensions

## 6.1 Top and Bottom Views of the Module

## 6.2 Mechanical Dimensions of the Module




## 6.3 Module Stand-off(PAN NUT)

The modules will need a mechanical retention at the end of the board. The module specifies a 5.5 mm diameter Keep-out zone at the end for attaching a screw. This section provides a guideline for using a M2 x 0.4 mm screw with a shoulder stand-off.

### 6.3.1 Recommended Main Board Hole

The recommended plated-hole sizes for the main board are:

- Drill size 4.3 mm
- Finish size 4.2 ±0.075 mm
- Pad size 6.5 mm

### 6.3.2 Electrical Ground Path

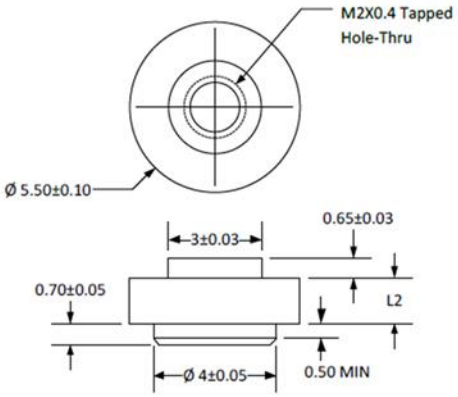
The module Stand-off and mounting screw also serve as part of the module Electrical Ground path.

The Stand-off should be connected directly to the ground plane on the platform. So that when the module is mounted and the mounting screw is screwed on to hold the module in place, this will make the electrical ground connection from the module to the platform ground plane.

### 6.3.3 Stand-off Guideline

A shoulder stand-off is a board-level SMT component that has a 2 x 0.4 thread. The height of the stand-off is determined by what connector is used.

* Our manual doesn't provide a flat stand-off




| Connector Height Descriptor | L2 |
|---|---|
| **H3.2** | 1.45 ± 0.03 |
| **H4.2** | 2.45 ± 0.03 |

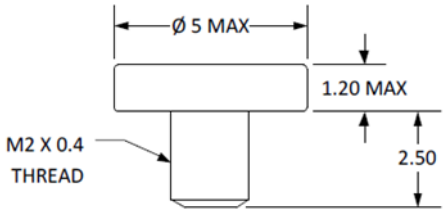
*L2 depends on your M.2 connector height.

- ✓ Requirements for SMT

- Polymide patch required for vacuum pick-up
- Minimum thermal conductivity of 50 W/(mK) or greater
- Material = Steel
- Finish = Matte tin, 1.2 microns minimum average
- Tape and reel

### 6.3.4 Screw Guideline

Screw consideration should be made to usage model. The tolerances of the connector, module and stand-off allow for a gap to exist between the seating plane and the contact.
the guidelines of a wafer-head style M2 screw are provided. This screw is intended for use only with the shouldered stand-off. The length is to be determined by the system design; 2 mm length supports L2=1.45 and 2.45 stand-off.




M2 SCREW-PHILLIPS DRIVE
WAFER HEAD STYLE
(USED WITH SHOULDER STAND 0FF)

# 7. Label

## 7.1 Label


## 7.2 Label Notations

- WM-H801SE
- 기기의 명칭: 5G 이동통신용 무선설비의 기기(기타)
- 인증번호
- 인증받은자의 상호: ㈜우리넷
- 제조자/제조국가: ㈜ 우리넷/한국
- 인증번호 : X※XXX-XX-XXXX
- 제조년원일: YYYY.MM.DD
- 일련번호: 0000000